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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/760,741	01/17/01	BROOKS J	M4065.0374/P

MM21/0814

THOMAS J. D'AMICO
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON DC 20037-1526

EXAMINER	
CHU, C	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 08/14/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/760,741	Brooks	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 39* is/are pending in the application.

4a) Of the above claim(s) *32 - 39* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's election without traverse of Group I in Paper No. 6 is acknowledged.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "22" has been used to designate both first adhesive layer and second adhesive layer; reference character "24" has been used to designate both cavity and adhesive fillet; and reference character "40" has been used to designate both wire bonds and third semiconductor dies. Correction is required.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: reference number "46" in Fig. 7 is not disclosed in the specification. Correction is required.

Specification

4. The disclosure is objected to because of the following informalities:

On page 6, line 11, "the top surface" should be --a top surface--.

On page 7, line 21, "the assembly 20" should be --the assembly 200--.

On page 8, line 16, "the balls" should be --balls--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1, 15, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsubonoya.

Note Fig. 6(A) of Tsubonoya, where the reference shows a semiconductor assembly comprising: a support structure (3) having a top surface (see Fig. 6(A)); and at least one semiconductor die (1a and 1b) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure (see Fig. 6(A)), said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material which does not extend past the perimeter of said at least one semiconductor die (see Fig. 1(A) and Fig. 6(A)).

Regarding claim 15, note Fig. 6(A) of Tsubonoya, where the reference shows a semiconductor assembly comprising: a first semiconductor die (1a) having a top and a bottom surface (see Fig. 6(A)); and a second semiconductor die (1b) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (see Fig. 6(A)), said second die being secured at its bottom surface to said top surface of said

first semiconductor die by a flowable adhesive material (see 15 in Fig. 1(A)) which does not extend past the perimeter of said second semiconductor die (see Fig. 6(A)).

Regarding claim 27, note Fig. 6(A) of Tsubonoya, where the reference shows a semiconductor assembly comprising: a support structure (3); a first semiconductor die (1a) having a top and bottom surface, said bottom surface being secured to said support structure (see Fig. 6(A)); and a second semiconductor die (1b) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (see Fig. 6(A)), said second die (1b) being secured at its bottom surface to said top surface of said first semiconductor die (1a) by a flowable adhesive material (15 in Fig. 1(A)) which does not extend past the perimeter of said second die (see Fig. 1(A)).

7. Claims 1, 15, and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Chin.

Note Fig. 2 of Chin, where the reference shows a semiconductor assembly comprising: a support structure (8) having a top surface (see Fig. 2); and at least one semiconductor die (7a and 7b) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure (see Fig. 2), said at least one semiconductor die (7b) being secured at its bottom surface to said top surface of said support structure (8) by a flowable adhesive material which does not extend past the perimeter of said at least one semiconductor die (see Fig. 2).

Regarding claim 15, note Fig. 2 of Chin, where the reference shows a semiconductor assembly comprising: a first semiconductor die (7b) having a top and a bottom surface (see Fig. 2); and a second semiconductor die (7a) having a top and bottom surface, said bottom surface

having a smaller area than said top surface of said first semiconductor die (see Fig. 2), said second die (7a) being secured at its bottom surface to said top surface of said first semiconductor die (7b) by a flowable adhesive material which does not extend past the perimeter of said second semiconductor die (see Fig. 2).

Regarding claim 27, note Fig. 2 of Chin, where the reference shows a semiconductor assembly comprising: a support structure (8); a first semiconductor die (7b) having a top and bottom surface, said bottom surface being secured to said support structure (see Fig. 2); and a second semiconductor die (7a) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (see Fig. 2), said second die (7a) being secured at its bottom surface to said top surface of said first semiconductor die (7b) by a flowable adhesive material which does not extend past the perimeter of said second die (see Fig. 2).

8. Claims 1 ~ 7, 10 ~ 19, 21, 27, 30, and 31 are rejected under 35 U.S.C. 102(e) as being anticipated by Fukui et al.

Note Fig. 1 of Fukui et al., where the reference shows a semiconductor assembly comprising: a support structure (5) having a top surface (see Fig. 1); and at least one semiconductor die (1 and 2) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure (see Fig. 1), said at least one semiconductor die (1) being secured at its bottom surface to said top surface of said support structure (5) by a flowable adhesive material (6) which does not extend past the perimeter of said at least one semiconductor die (see Fig. 1).

Regarding claims 2 and 17, note Fig. 1 of Fukui et al., where the reference shows said support structure (5) is a film (see Fig. 2(a)).

Regarding claims 3 and 18, since Fukui et al. does not limit the circuit board to any particular or specific device, the reference encompasses all well known circuit board's including "printed circuit board."

Regarding claim 4, note Fig. 1 of Fukui et al., where the reference shows said support structure is at least one semiconductor die (1) with a top and bottom surface (see Fig. 1).

Regarding claims 5 and 19, Fukui et al. discloses said flowable adhesive material (6 in Fig. 1) is an epoxy (column 9, lines 15 ~ 17).

Regarding claim 6, note Figs. 11(a) ~ 11(g) of Fukui et al., where the reference shows said flowable adhesive material (24) covers an area less than or equal to about 90% of said at least one semiconductor die bottom surface area (see Fig. 11(b)).

Regarding claim 7, note Fig. 1 of Fukui et al., where the reference shows said flowable adhesive material (6) covers an area greater than or equal to about 50% of said at least one semiconductor die bottom surface area (see Fig. 1).

Regarding claim 10, note Fig. 1 of Fukui et al., where the reference shows said at least one semiconductor die (1) is in electrical communication with at least one electrical contact area provided on said support structure (see Fig. 1).

Regarding claim 11, note Fig. 1 of Fukui et al., where the reference shows said electrical communication is through a wire bond (7 in Fig. 1).

Regarding claim 12, note Fig. 1 of Fukui et al., where the reference shows said at least one electrical contact area is a bonding pad (see Fig. 1).

Regarding claim 13, note Fig. 1 of Fukui et al., where the reference shows further comprising an encapsulating material (8) for encapsulating said die, electrical communication, and at least a portion of said support structure (see Fig. 1).

Regarding claim 14, note Figs. 11(a) ~ 11(g) of Fukui et al., where the reference shows said encapsulating material fills (8) in at least some portion of a space between said bottom surface of said die (21) and said top surface of said support structure (see Fig. 11(g)).

Regarding claim 15, note Fig. 1 of Fukui et al., where the reference shows a semiconductor assembly comprising: a first semiconductor die (1) having a top and a bottom surface (see Fig. 1); and a second semiconductor die (2) having a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (see Fig. 1), said second die (2) being secured at its bottom surface to said top surface of said first semiconductor die (1) by a flowable adhesive material (6) which does not extend past the perimeter of said second semiconductor die (see Fig. 1).

Regarding claim 16, note Fig. 1 of Fukui et al., where the reference shows said first semiconductor die (1) is secured to a support structure (see Fig. 1).

Regarding claim 21, note Fig. 1 of Fukui et al., where the reference shows said flowable adhesive material (6) covers an area greater than or equal to about 50% of said second semiconductor die's bottom surface area (see Fig. 1).

Regarding claim 27, note Fig. 1 of Fukui et al., where the reference shows a semiconductor assembly comprising: a support structure (5); a first semiconductor die (1) having a top and bottom surface, said bottom surface being secured to said support structure (see Fig. 1); and a second semiconductor die (2) having a top and bottom surface, said bottom surface having

a smaller area than said top surface of said first semiconductor die (see Fig. 1), said second die (2) being secured at its bottom surface to said top surface of said first semiconductor die (1) by a flowable adhesive material (6) which does not extend past the perimeter of said second die (see Fig. 1).

Regarding claim 30, note Fig. 1 of Fukui et al., where the reference shows at least one of said first and said second semiconductor dies (1 and 2) are in electrical communication with said support structure (see Fig. 1).

Regarding claim 31, note Fig. 7(b) of Fukui et al., where the reference shows said second semiconductor die (2) is in electrical communication with an electrical contact area (17a) on said first semiconductor die (see Fig. 7(b)).

9. Claims 22 ~ 24 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Hawke et al.

Note Fig. 5 of Hawke et al., where the reference shows a semiconductor assembly comprising: a first semiconductor die (216) having a top and a bottom surface (see Fig. 5); and a second semiconductor die (218a) having a top and a bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (see Fig. 5); a third semiconductor die (218b) having a top and a bottom, said bottom surface having a smaller area than said top surface of said first semiconductor die (see Fig. 5), said second and third semiconductor dies being secured at their bottom surface to said top surface of said first semiconductor die by a flowable adhesive material which does not extend past the perimeter of

said second semiconductor die or said third semiconductor die (see Fig. 5 and column 12, lines 32 ~ 39).

Regarding claim 23, note Fig. 5 of Hawke et al., where the reference shows said bottom surface of said first semiconductor die (261) is secured to a support structure (see Fig. 4 and Fig. 5).

Regarding claim 24, Hawke et al. discloses said flowable adhesive material is an epoxy (column 12, lines 32 ~ 33).

Regarding claim 26, Hawke et al. discloses said flowable adhesive material covers an area greater than or equal to about 50% of said second and said third semiconductor die's bottom surface area (read column 12, lines 32 ~ 39).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 8, 9, 20, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui et al. in view of Ball.

Regarding claims 8, 9, 28, and 29, Fukui et al. discloses the claimed invention except for a distance between an electrical contact area and said perimeter of said at least one

semiconductor die is less than or equal to about 200 microns. However, Ball shows that said top surface of a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns (see Fig. 2). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Fukui et al. by including a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 200 microns as taught by Ball. The ordinary artisan would have been motivated to modify Fukui et al. in the manner described above for at least the purpose of decreasing a size of the package.

Regarding claim 20, Fukui et al. discloses the claimed invention except for said flowable adhesive material covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area. However, Ball shows that said flowable adhesive material (22) covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area (see Fig. 2). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Fukui et al. by including said flowable adhesive material covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area as taught by Ball. The ordinary artisan would have been motivated to modify Fukui et al. in the manner described above for at least the purpose of eliminating overflow of the adhesive agent between the first and second semiconductor chip.

12. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hawke et al. in view of Ball.

Hawke et al. discloses the claimed invention except for said flowable adhesive material covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area. However, Ball shows that said flowable adhesive material (22) covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area (see Fig. 2). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Hawke et al. by including said flowable adhesive material covers an area less than or equal to about 90% of said second semiconductor die's bottom surface area as taught by Ball. The ordinary artisan would have been motivated to modify Hawke et al. in the manner described above for at least the purpose of increasing packaging density.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Juso et al. and JP P2001-94045A disclose a plurality of semiconductor chips package.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7382 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
August 10, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800